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(71) Applicant *(for all designated States except US)*: **LG INNOTEK CO., LTD** [KR/KR]; 14th Fl. Hansol Bldg., 736-1, Yoksam-dong, Kangnam-gu, Seoul 135-983 (KR).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **LEE, Suk Hun** [KR/KR]; Line7th Apt.706-502, Wolgae-dong, Gwangsan-gu, Gwangju 506-302 (KR).

(74) Agent: **HAW, Yong Noke**; 8th Fl. Songchon Bldg., 642-15 Yoksam-dong, Kangnam-gu, Seoul 135-080 (KR).

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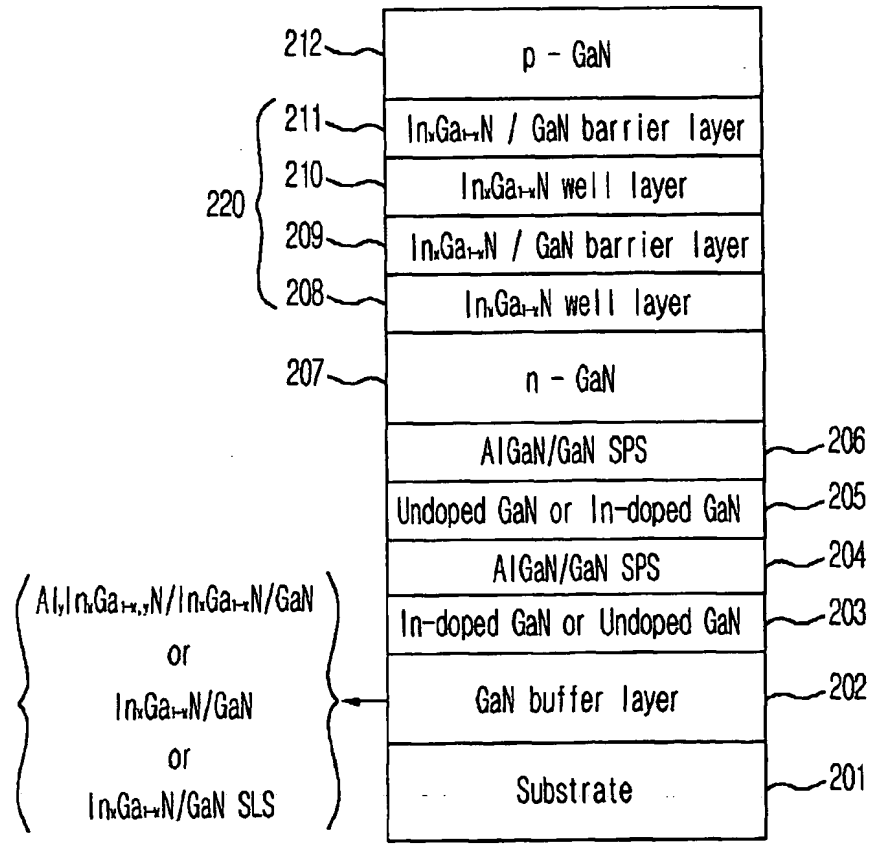

(57) Abstract: Disclosed a nitride semiconductor LED including: a substrate; a GaN-based buffer layer formed on the substrate; $Al_yGa_{1-y}N$/GaN short period superlattice (SPS) layers formed on the GaN-based buffer layer in a sandwich structure of upper and lower parts having an undoped GaN layer or an indium-doped GaN layer interposed therebetween (Here, $0 \leq y \leq 1$); a first electrode layer of an n-GaN layer formed on the upper $Al_yGa_{1-y}N$/GaN SPS layer; an active layer formed on the first electrode layer; and a second electrode layer of a p-GaN layer formed on the active layer.

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NITRIDE SEMICONDUCTOR LED AND FABRICATION METHOD THEREOF

Technical Field

The present invention relates to a nitride semiconductor, and more particularly, to a GaN-based nitride semiconductor light emitting device (LED) and a fabrication method thereof.

Background Art

Generally, a GaN-based nitride semiconductor is applied to electronic devices that are high-speed switching and high power devices such as optic elements of blue/green LEDs, MESFET, HEMT, etc. In particular, the blue/green LED is under a state in which mass-production has been already progressed and a global sale is being exponentially increased.

The above-mentioned conventional GaN-based nitride semiconductor light emitting device (LED) is grown-up usually on a sapphire substrate or a SiC substrate. Further, at a low growth temperature, an $Al_yGa_{1-y}N$ polycrystalline layer is grown-up on the sapphire substrate or the SiC substrate as a buffer layer. After that, at a high temperature, an undoped GaN layer, an n-GaN layer doped with silicon over a $1\times10^{17}/cm^3$ concentration or a combined n-GaN layer thereof is formed on the buffer layer as a first electrode layer. Additionally, on an Mg-AlGaN cladding layer is formed an Mg-GaN layer as a second electrode layer to complete the GaN-based nitride semiconductor LED. Also, a light emitting layer (multi-quantum well active layer) is sandwiched between the first electrode layer and the second electrode layer.

However, the above-constructed conventional nitride semiconductor LED has a crystal defect of a very high

value of about $10^8/cm^2$ or so, which is generated from an interface between the substrate and the buffer layer.

Accordingly, the conventional nitride semiconductor LED has a drawback in that an electric characteristic, specifically, leakage current under a reverse bias condition is increased, resulting in a fatal influence to the reliability of the device.

Also, the conventional nitride semiconductor LED has another drawback in that the crystal defect generated from the interface between the buffer layer and the substrate deteriorates crystallinity of the light emitting layer thereby lowering the light emitting efficiency.

Disclosure of the Invention

An object of the present invention is to provide a nitride semiconductor LED and a fabrication method thereof for reducing a crystal defect generated due to a difference in a thermal expansion coefficient and a lattice constant between a substrate and a GaN-based single crystalline layer grown-up on the substrate, and improving crystallinity of the GaN-based single crystalline layer, to thereby improve the performance of the device and assure the reliability.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, there is provided a nitride semiconductor LED including: a substrate; a GaN-based buffer layer formed on the substrate; $Al_yGa_{1-y}N/GaN$ short period superlattice (SPS) layers formed on the GaN-based buffer layer in a sandwich structure of upper and lower parts having an undoped GaN layer or an indium-doped GaN layer interposed therebetween (Here, $0 \leq y \leq 1$); a first electrode layer of an n-GaN layer formed on the

upper $Al_yGa_{1-y}N$/GaN SPS layer; an active layer formed on the first electrode layer; and a second electrode layer of a p-GaN layer formed on the active layer.

According to another aspect of the present invention, there is provided a nitride semiconductor LED, including: a substrate; a GaN-based buffer layer formed on the substrate; a first electrode layer of an n^+-GaN layer formed on the GaN-based buffer layer and containing a high concentration of dopants; an n-GaN layer formed on the first electrode layer and containing a low concentration of dopants; an active layer formed on the n-GaN layer; and a second electrode layer of a p-GaN layer formed on the active layer.

According to still another aspect of the present invention, there is provided a fabrication method of a nitride semiconductor LED, the method including the steps of: growing-up a GaN-based buffer layer on a substrate; forming $Al_yGa_{1-y}N$/GaN short period superlattice (SPS) layers on the GaN-based buffer layer in a sandwich structure of upper and lower parts having an undoped GaN layer or an indium-doped GaN layer interposed therebetween (Here, $0 \leq y \leq 1$); forming a first electrode layer of an n^+-GaN layer containing a high concentration of dopants, on the upper $Al_yGa_{1-y}N$/GaN SPS layer; forming an active layer on the first electrode layer; and forming a second electrode layer of an p-GaN layer on the active layer.

Brief Description of the Drawings

FIG. 1 is a sectional view illustrating a schematic construction of a nitride semiconductor LED according to a first embodiment of the present invention;

FIG. 2 is a sectional view illustrating a schematic construction of a nitride semiconductor LED according to

a second embodiment of the present invention; and

FIG. 3 is a sectional view illustrating a schematic construction of a nitride semiconductor LED according to a third embodiment of the present invention.

Best Mode for Carrying Out the Invention

Hereinafter, preferred embodiments of the present invention will be described in detail with reference to accompanying drawings.

FIG. 1 is a sectional view illustrating a schematic construction of a nitride semiconductor LED according to a first embodiment of the present invention.

Referring to FIG. 1, the inventive nitride semiconductor LED includes a substrate 101; a GaN-based buffer layer 102 formed on the substrate 101; a first electrode layer of an n-GaN layer 105 formed on the GaN-based buffer layer 102; an active layer 120 formed on the first electrode layer; and a second electrode layer of a p-GaN layer 110 formed on the active layer 120.

Herein, the GaN-based buffer layer 102 can be formed having a triple-structured $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N/GaN$ (Here, $0 \leq x \leq 1$, $0 \leq y \leq 1$) laminated, a double-structured $In_xGa_{1-x}N/GaN$ (Here, $0 \leq x \leq 1$) laminated, or a super-lattice-structured (SLS) $In_xGa_{1-x}N/GaN$ (Here, $0 \leq x \leq 1$) laminated.

In other words, in the inventive nitride semiconductor LED, on the substrate 101 (for example, a sapphire substrate or a SiC substrate) is grown-up the GaN-based nitride semiconductor as the GaN-based buffer layer 102, the n-GaN layer 105 is formed as the first electrode layer, and an atomic Mg-doped p-GaN layer 110 is formed as the second electrode layer. Additionally, the active layer 120 having an InGaN/GaN multi-quantum well structure is formed in a sandwich combination

structure between the first electrode layer of the n-GaN layer 105 and the second electrode layer of the p-GaN layer 110.

Here, the active layer 120 can be formed with an $In_xGa_{1-x}N$ well layer 106, an $In_xGa_{1-x}N$/GaN barrier layer 107, an $In_xGa_{1-x}N$ well layer 108 and an $In_xGa_{1-x}N$/GaN barrier layer 109. Further, between the GaN-based buffer layer 102 and the first electrode layer of the n-GaN layer 105 can be also additionally formed an undoped GaN layer or an indium-doped GaN layer 103 and 104.

Additionally, in a process of growing-up the GaN-based buffer layer 102 on the substrate 101 at a low temperature, a metal organic chemical vapor deposition (MOCVD) equipment is used such that it is, in a growth pressure of 100-700torr and at a low temperature of 500-800℃, grown-up to have a thickness of below 700Å in a laminated structure such as the triple-structured $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N$/GaN, the double-structured $In_xGa_{1-x}N$/GaN or the super-lattice-structured (SLS) $In_xGa_{1-x}N$/GaN, etc.

At this time, for growing-up the GaN-based buffer layer 102 at the low temperature, the MOCVD equipment is used having a carrier gas of H2, N2 supplied while a source gas of TMGa, TMIn, TMAl introduced and simultaneously a NH_3 gas introduced.

Further, in a high temperature process of growing-up the GaN-based single crystalline layer, on the GaN-based buffer layer 102 is, at a 900-1100℃ temperature, the undoped GaN layer or the indium-doped GaN layer 103 and 104, and on the result thereof is again formed an atomic silicon-doped n-GaN layer 105 (over a $1x10^{18}/cm^3$ concentration). Herein, the n-GaN layer 105 is used as the first electrode layer and has a carrier concentration of over $1x10^{18}/cm^3$.

At this time, for growing-up the GaN-based single crystalline layer, the MOCVD equipment is used having the source gas of TMGa, TMIn supplied at the 900-1100℃ temperature to grow-up the GaN-based single crystalline layer. Additionally, the TMGa, TMIn source gas is introduced for supplying at the 100-700torr pressure and a 0.1-700 μmol/min flow rate to grow-up the GaN-based single crystalline layer. At this time, a SiH_4 gas is used as a dopant gas for doping a silicon atom.

On the other hand, FIG. 2 is a sectional view illustrating a schematic construction of a nitride semiconductor LED according to a second embodiment of the present invention.

Referring to FIG. 2, in the inventive nitride semiconductor LED, on the substrate 201 (for example, the sapphire substrate or the SiC substrate) is provided the GaN-based buffer layer 202 having the triple-structured $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N/GaN$ (Here, $0 \leq x \leq 1$, $0 \leq y \leq 1$), the double-structured $In_xGa_{1-x}N/GaN$ (Here, $0 \leq x \leq 1$), or the super-lattice-structured (SLS) $In_xGa_{1-x}N/GaN$ (Here, $0 \leq x \leq 1$). Additionally, on the GaN-based buffer layer 202 is formed the undoped GaN layer or the indium-doped GaN layer 203.

Further, on the undoped GaN layer or the indium-doped GaN layer 203 are formed $Al_yGa_{1-y}N/GaN$ SPS layers 204 and 206 in a sandwich structure of upper and lower parts having the undoped GaN layer or the indium-doped GaN layer 205 interposed therebetween.

On the upper $Al_yGa_{1-y}N/GaN$ SPS layer 206 is formed the n-GaN layer 207 as the first electrode layer. Here, the first electrode layer of the n-GaN layer 207 has the carrier concentration of over $1x10^{18}/cm^3$, and has the silicon used as the dopant.

Additionally, the nitride semiconductor LED

includes, as a light emitting layer, an active layer 220 of $In_xGa_{1-x}N/GaN$. Here, the active layer 220 can be formed in the multi-quantum well structure having an $In_xGa_{1-x}N$ well layer 208, an $In_xGa_{1-x}N/GaN$ barrier layer 209, an $In_xGa_{1-x}N$ well layer 210 and an $In_xGa_{1-x}N/GaN$ barrier layer 211.

In the present invention, when the active layer 220 is formed, the $In_xGa_{1-x}N$ well layers 208 and 210 and the $In_xGa_{1-x}N/GaN$ barrier layers 209 and 211 are grown-up to respectively have a thickness of less than 70Å at a 700-800℃ growth temperature and in a N_2 atmosphere. After that, the growth temperature is increased to a range of 900-1020 ℃ and a Cp_2Mg doping gas is introduced so that a p-GaN layer 212 is grown-up in a 0.01-0.5㎛ thickness to be used as a second electrode layer, and at this time, a mixed gas atmosphere of NH_3, H_2 as atmosphere gas is maintained with a high purity degree.

At this time, as shown in FIG. 2, the inventive nitride semiconductor LED includes the $Al_yGa_{1-y}N/GaN$ SPS layers 204 and 206. Accordingly, in order to evaluate an influence of the sandwich-structured $Al_yGa_{1-y}N/GaN$ SPS layers 204 and 206 upon a crystallinity variation, a structure is grown-up not including the $In_xGa_{1-x}N/GaN$ multi-quantum well structure of the active layer 220 and the second electrode layer of the p-GaN layer 212, and then a DC-XRD analysis is performed.

As a result of the above DC-XRD analysis, in case of a conventional nitride semiconductor having an undoped GaN/n-GaN structure as the buffer layer, a FWHM (full-width half-maximum) value of about 290 arcsec is obtained, but in case of having the inventive structure of FIG. 2, a FWHM value of about 250 arcsec is obtained. Considering the above, in case of having the sandwich-structured $Al_yGa_{1-y}N/GaN$ SPS layers 204 and 206 as in the

present invention, it can be appreciated that the crystallinity is improved.

Furthermore, as a result of analyzing an electrical characteristic of the nitride semiconductor LED having the structure of FIG. 2, a forward bias characteristic such as an operation voltage (VF) and the brightness, etc. is not varied. However, it can be appreciated that, when the reverse bias is applied, a conventional reverse bias breakdown voltage is increased from "-15V" to over "-19V" so that the current leakage is improved.

The above-improved characteristic is caused by an effect of effectively reducing a dislocation formed in the substrate 201 and the GaN-based buffer layer 202 to be intruded into surface. And accordingly, it is caused by the result that the $In_xGa_{1-x}N$/GaN multi-quantum well structure of the active layer 220 and the p-GaN layer 212 are improved in their crystallinities.

On the other hand, the present invention provides, for more improving the characteristic, the nitride semiconductor LED having the following structure.

FIG. 3 is a sectional view illustrating a schematic construction of the nitride semiconductor LED according to a third embodiment of the present invention.

As shown in FIG. 3, in the inventive nitride semiconductor LED, on a first electrode layer of a high concentration doped n^+-GaN layer 307 is additionally grown-up a low concentration silicon of about $1x10^{17}/cm^3$ doped n-GaN layer 308. Accordingly, in an interface of the $In_xGa_{1-x}N$ well layer 309 grown-up first in the $In_xGa_{1-x}N$/GaN multi-quantum well structured active layer 320 grown-up at a relatively low growth temperature, a stress can be suppressed and crystallinity can be improved.

Here, in case the n-GaN layer 308 is formed with a semi-insulating GaN layer, it can also function as a role

of a current prevention layer for effectively cutting off the current leakage which is, at the time of reverse bias, reversely intruded in the light emitting layer (multi-quantum well active layer).

Additionally describing, in case the nitride semiconductor LED is reversely biased, its crystallinity deterioration results in the current leakage. Accordingly, for preventing this, it can be formed in a structure having a thin semi-insulating GaN layer or a low concentration of below $1x10^{18}/cm^3$ doped n-GaN layer inserted.

In other words, the inventive nitride semiconductor LED includes a substrate 301; a GaN-based buffer layer 302 formed on the substrate 301; a first electrode layer of an n^+-GaN layer 307 formed on the GaN-based buffer layer 302 and containing a high concentration of dopants; an n-GaN layer 308 formed on the first electrode layer and containing a low concentration of dopants; an active layer 320 formed on the n-GaN layer 308; and a second electrode layer of a p-GaN layer 313 formed on the active layer 320.

Here, on the substrate 301 is provided the GaN-based buffer layer 302 having the triple-structured $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N/GaN$ (Here, $0 \leq x \leq 1$, $0 \leq y \leq 1$), the double-structured $In_xGa_{1-x}N/GaN$ (Here, $0 \leq x \leq 1$) or the super-lattice-structured (SLS) $In_xGa_{1-x}N/GaN$ (Here, $0 \leq x \leq 1$). Additionally, on the GaN-based buffer layer 302 is formed an undoped GaN layer or an indium-doped GaN layer 303.

Further, on the undoped GaN layer or the indium-doped GaN layer 303 are formed $Al_yGa_{1-y}N/GaN$ SPS layers 304 and 306 in a sandwich structure of upper and lower parts having the indium-doped GaN layer 305 interposed therebetween.

On the upper $Al_yGa_{1-y}N$/GaN SPS layer 306 is formed the n^+-GaN layer 307 as the first electrode layer. Here, the first electrode layer of the n^+-GaN layer 307 has the carrier concentration of over $1x10^{18}/cm^3$ and has silicon used as the dopant.

Additionally, the nitride semiconductor LED includes, as the light emitting layer, the active layer 320 of $In_xGa_{1-x}N$/GaN. Here, the active layer 320 can be formed to have the multi-quantum well structure having an $In_xGa_{1-x}N$ well layer 309, an $In_xGa_{1-x}N$/GaN barrier layer 310, an $In_xGa_{1-x}N$ well layer 311 and an $In_xGa_{1-x}N$/GaN barrier layer 312.

On the other hand, in a fabrication method of the nitride semiconductor LED according to the present invention, when the undoped GaN layer and the indium-doped GaN layer 305 and 306, and the first electrode layer of the n^+-GaN layer 307 are grown-up, besides a high purity degree of NH_3 and H_2 carrier gases, a N_2 gas is mixed and used as the carrier gas. In the above-processed case, a thickness regularity doped and grown-up is improved. Additionally, from analysis of a forward and reverse electrical characteristic, an operation voltage and a reverse breakdown voltage can be obtained having a very regular dispersion distribution in a wafer.

Industrial Applicability

As described above, the inventive semiconductor LED and its fabrication method can reduce the crystal defect caused by the difference of the thermal expansion coefficient and the lattice constant in the substrate and the GaN-based single crystalline layer grown-up on the substrate, and can improve the GaN-based single crystalline layer in its crystallinity. Accordingly, the present invention has an advantage in which the nitride

semiconductor LED can be improved in its performance and assured in its reliability.

Claims

1. A nitride semiconductor LED, comprising:

a substrate;

a GaN-based buffer layer formed on the substrate;

$Al_yGa_{1-y}N/GaN$ short period superlattice (SPS) layers formed on the GaN-based buffer layer in a sandwich structure of upper and lower layers having an undoped GaN layer or an indium-doped GaN layer interposed therebetween (where, $0 \leq y \leq 1$);

a first electrode layer of an n-GaN layer formed on the upper $Al_yGa_{1-y}N/GaN$ SPS layer;

an active layer formed on the first electrode layer; and

a second electrode layer of a p-GaN layer formed on the active layer.

2. The nitride semiconductor LED of claim 1, wherein the GaN-based buffer layer has a triple-structured $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N/GaN$ laminated (Here, $0 \leq x \leq 1$, $0 \leq y \leq 1$), a double-structured $In_xGa_{1-x}N/GaN$ laminated (Here, $0 \leq x \leq 1$), or a super-lattice-structured (SLS) $In_xGa_{1-x}N/GaN$ laminated (Here, $0 \leq x \leq 1$).

3. The nitride semiconductor LED of claim 1, further comprising the undoped GaN layer or the indium-doped GaN layer on the GaN-based buffer layer.

4. A nitride semiconductor LED, comprising:

a substrate;

a GaN-based buffer layer formed on the substrate;

an undoped GaN layer or an indium-doped GaN layer formed on the GaN-based buffer layer;

$Al_yGa_{1-y}N/GaN$ short period superlattice (SPS) layers

formed on the undoped GaN layer or the indium-doped GaN layer, in a sandwich structure of upper and lower layers having the undoped GaN layer or the indium-doped GaN layer interposed therebetween (Here, $0 \leq y \leq 1$);

a first electrode layer of an n^+-GaN layer formed on the upper $Al_yGa_{1-y}N$/GaN SPS layer and containing a high concentration of dopants;

an n-GaN layer formed on the first electrode layer and containing a low concentration of dopants;

an active layer formed on the n-GaN layer; and

a second electrode layer of a p-GaN layer formed on the active layer.

5. The nitride semiconductor LED of claim 4, wherein the GaN-based buffer layer has a triple-structured $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N$/GaN laminated (Here, $0 \leq x \leq 1$, $0 \leq y \leq 1$), a double-structured $In_xGa_{1-x}N$/GaN laminated (Here, $0 \leq x \leq 1$), or a super-lattice-structured (SLS) $In_xGa_{1-x}N$/GaN laminated (Here, $0 \leq x \leq 1$).

6. A nitride semiconductor LED, comprising:

a substrate;

a GaN-based buffer layer formed on the substrate;

a first electrode layer of an n^+-GaN layer formed on the GaN-based buffer layer and containing a high concentration of dopants;

an n-GaN layer formed on the first electrode layer and containing a low concentration of dopants;

an active layer formed on the n-GaN layer; and

a second electrode layer of a p-GaN layer formed on the active layer.

7. The nitride semiconductor LED of claim 6, wherein the dopant concentration of the n^+-GaN layer is

more than $1x10^{18}/cm^3$.

8. The nitride semiconductor LED of claim 6, wherein the dopant concentration of the n-GaN layer is less than $1x10^{18}/cm^3$.

9. The nitride semiconductor LED of claim 6, wherein the dopant concentration of the n-GaN layer is $1x10^{17}/cm^3$.

10. The nitride semiconductor LED of claim 6, wherein the GaN-based buffer layer has a triple-structured $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N/GaN$ laminated (Here, $0 \leq x \leq 1$, $0 \leq y \leq 1$), a double-structured $In_xGa_{1-x}N/GaN$ laminated (Here, $0 \leq x \leq 1$), or a super-lattice-structured (SLS) $In_xGa_{1-x}N/GaN$ laminated (Here, $0 \leq x \leq 1$).

11. The nitride semiconductor LED of claim 6, further comprising $Al_yGa_{1-y}N/GaN$ short period superlattice (SPS) layers formed on the GaN-based buffer layer in a sandwich structure of upper and lower parts having an undoped GaN layer or an indium-doped GaN layer interposed therebetween (Here, $0 \leq y \leq 1$).

12. A fabrication method of a nitride semiconductor LED, the method comprising the steps of:

growing-up a GaN-based buffer layer on a substrate;

forming $Al_yGa_{1-y}N/GaN$ short period superlattice (SPS) layers on the GaN-based buffer layer in a sandwich structure of upper and lower parts having an undoped GaN layer or an indium-doped GaN layer interposed therebetween (Here, $0 \leq y \leq 1$);

forming a first electrode layer of an n^+-GaN layer containing a high concentration of dopants, on the upper

$Al_yGa_{1-y}N$/GaN SPS layer;

forming an active layer on the first electrode layer; and

forming a second electrode layer of an p-GaN layer on the active layer.

13. The fabrication method of claim 12, further comprising the step of forming an n-GaN layer containing a low concentration of dopants, between the first electrode layer of the n^+-GaN layer and the active layer.

14. The fabrication method of claim 12, wherein the GaN-based buffer layer is, using a MOCVD equipment, grown-up to have a 50-800Å thickness at a 500-800℃ temperature and in an atmosphere having H_2 and N_2 carrier gases supplied while having TMGa, TMIn, TMAl source gas introduced and simultaneously having NH_3 gas introduced.

15. The fabrication method of claim 12, wherein the GaN-based buffer layer is grown-up with a 5-300μmol/min flow rate of the TMGa, TMIn, TMAl source gas and a 100-700torr growth pressure.

16. The fabrication method of claim 12, wherein the GaN-based buffer layer has a triple-structured $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N$/GaN laminated (Here, $0 \leq x \leq 1$, $0 \leq y \leq 1$), a double-structured $In_xGa_{1-x}N$/GaN laminated (Here, $0 \leq x \leq 1$), or a super-lattice-structured (SLS) $In_xGa_{1-x}N$/GaN laminated (Here, $0 \leq x \leq 1$).

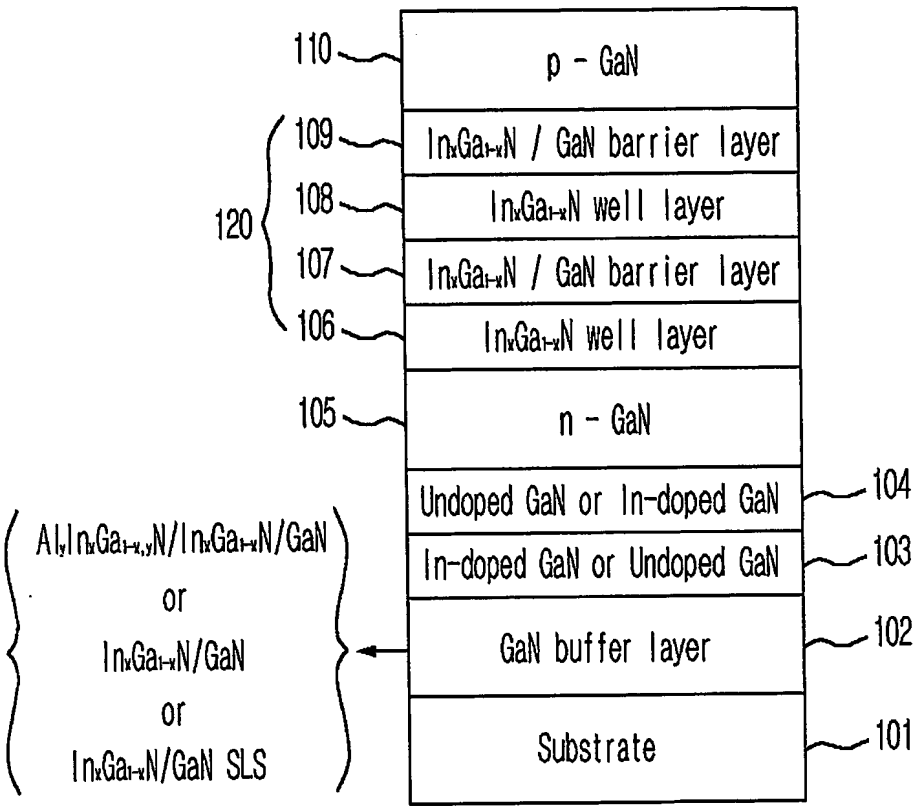
17. The fabrication method of claim 12, further comprising the step of forming an undoped GaN layer or an indium-doped GaN layer on the GaN-based buffer layer.

18. The fabrication method of claim 12, wherein the dopant concentration of the n^+-GaN layer is more than $1x10^{18}/cm^3$.

19. The fabrication method of claim 13, wherein the dopant concentration of the n-GaN layer is $1x10^{17}/cm^3$.

20. The fabrication method of claim 13, wherein the n-GaN layer is formed with a semi-insulating layer.

[FIG. 1]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Substrate
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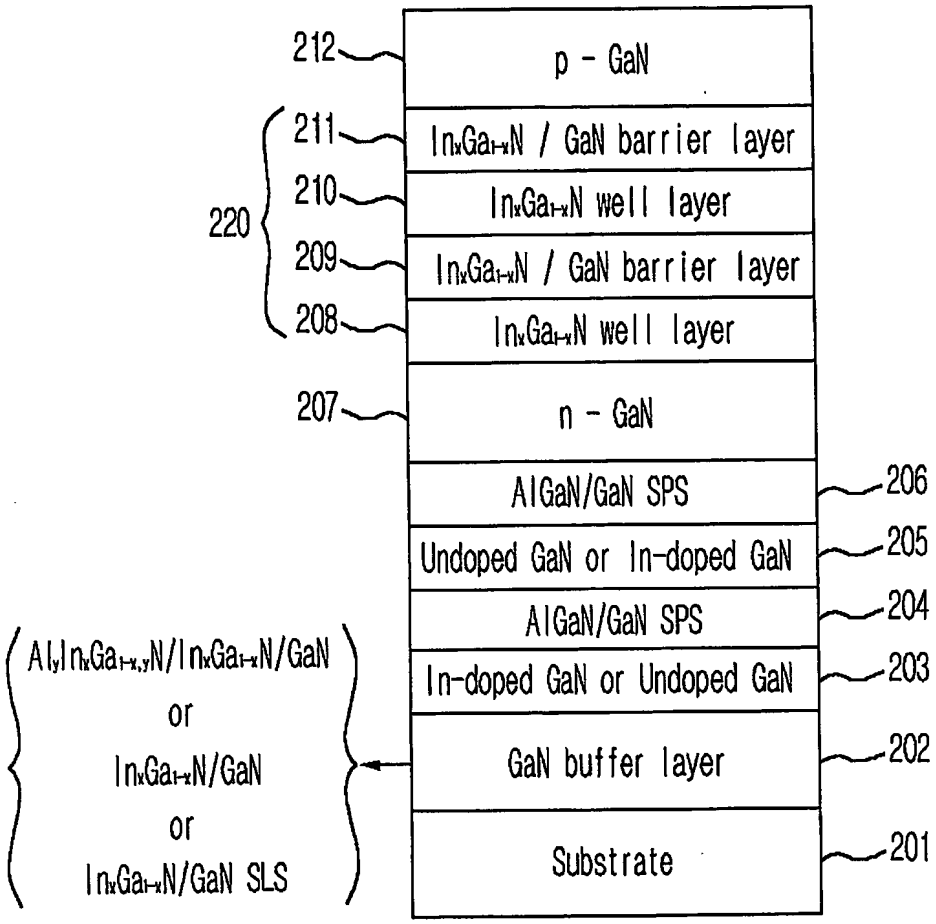
[FIG. 2]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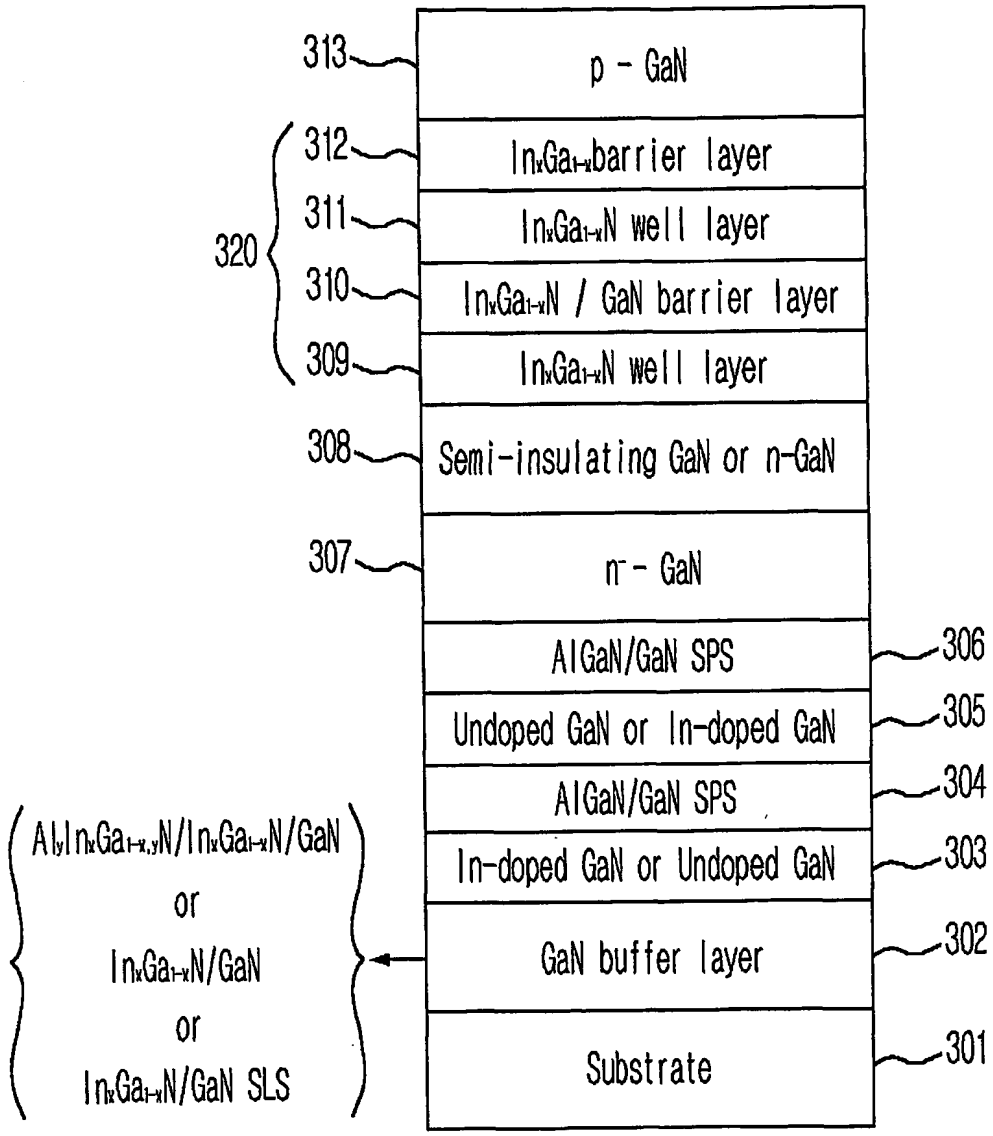
Undoped GaN or In-doped GaN
205
AlGaN/GaN SPS
204
In-doped GaN or Undoped GaN
203
GaN buffer layer
202
Substrate
201
AlyInxGa1-x,yN/InxGa1-xN/GaN
or
InxGa1-xN/GaN
or
InxGa1-xN/GaN SLS

[FIG. 3]


313
p - GaN
312
InxGa1-xbarrier layer
311
InxGa1-xN well layer
320
310
InxGa1-xN / GaN barrier layer
309
InxGa1-xN well layer
308
Semi-insulating GaN or n-GaN
307
n- - GaN
AlGaN/GaN SPS
306
Undoped GaN or In-doped GaN
305
AlGaN/GaN SPS
304
In-doped GaN or Undoped GaN
303
GaN buffer layer
302
Substrate
301
AlyInxGa1-x-yN/InxGa1-xN/GaN
or
InxGa1-xN/GaN
or
InxGa1-xN/GaN SLS

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR03/01668

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to part of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Search Authority found multiple inventions in this international application, as follows:

I. Claims 1-5 and 11-20 directed to a intermediate layer between a buffer layer and an n-clad layer of GaN-based LED.
II. Claims 6-10 directed to an n-clad layer of GaN-based LED

1. ☐ As all required addtional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☒ As all searchable claims could be established without effort justifying an additional fee, this Authority did not invite payment of any addition fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR03/01668

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 H01L 33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L H01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean patents and applications for inventions, since 1975

Electronic data base consulted during the internationl search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 9-153643 A2 (TOYODA GOSEI KK, TOYODA CHUO KENKYUSHO KK) 10 JUNE 1997 see the paragraph [0010]-[0012], Figure 1	6-9
A	see the whole documents	1-5, 10-20
A	JP 9-129925 A2 (TOYODA GOSEI KK, AKASAKI ISAMU, AMANO HIROSHI) 16 MAY1997 see the paragraph [0010]-[0011], Figure 1	1 -20
A	JP 2001-7397 A2 (NICHIA CHEM. IND. LTD) 12 JANUARY 2001 see the whole documents	1 -20
A	JP 10-173220 A2 (ROHM CO. LTD) 26 JULY 1998 see the whole documents	1 -20
A	JP 7-302929 A2 (SUMITOMO CHEM. CO. LTD) 14 NOVEMBER 1995 see the whole documents	1 -20
A	JP 7- 254733 A2 (NICHIA CHEM. IND. LTD) 3 OCTOBER 1995 see the Figure 3	1 -20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 NOVEMBER 2003 (24.11.2003)	24 NOVEMBER 2003 (24.11.2003)

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
920 Dunsan-dong, Seo-gu, Daejeon 302-701,
Republic of Korea
Facsimile No. 82-42-472-7140

Authorized officer
KIM, Dong Yup
Telephone No. 82-42-481-5749

INTERNATION[redacted]SEARCH REPORT
Information on patent family members

[redacted]ational application No.
PCT/KR03/01668

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 9-153643 A2	10.06.1997	NONE	
JP 9-129925 A2	16.05.1997	NONE	
JP 2001-7397 A2	12.01.2001	JP 3412563 B2	03.06.2003
JP 10-173220 A2	26.06.1998	NONE	
JP 7-302929 A2	14.11.1995	NONE	
JP 7- 254733 A2	03.10.1995	JP 3180871 B2	25.06.2001